CLAIMS

[1] A delta-sigma type fraction division PLL synthesizer comprising: a voltage controlled oscillator; a variable divider that has a division ratio switchable between M (M is a positive integer), (M+1), and (M-1) and performs frequency dividing of an output signal of said voltage controlled oscillator; a phase comparator for performing phase comparison of an output signal of said variable divider with a reference signal; a filter for smoothing an output signal of said phase comparator and then providing the signal to said voltage controlled oscillator; a first L-value accumulator (L is a positive integer) for accumulating a value K1 (K1 is an integer); a second L-value accumulator for accumulating a value K2 (K2 is an integer); and a first adder for subtracting an overflow signal of said second L-value accumulator from an overflow signal of said first L-value accumulator, wherein

said value K1 and K2 are set into values that satisfy K1-K2=K and have absolute values larger than a value K (K is an integer), while an output signal of said first adder is provided as a division ratio switching signal to said variable divider, so that when the output signal of said first adder has a zero value, the division ratio of said variable divider is set into M, while when the output signal of said first adder has a positive value, the division ratio of said variable divider is set into M+1, and while when the output signal of said first adder has a negative

value, the division ratio of said variable divider is set into M-1.

[2] A delta-sigma type fraction division PLL synthesizer according to claim 1, wherein the first L-value accumulator comprises: a first L-value adder that receives the value K1 (K1 is an integer) as one input; and a first data latch that holds an output of said first L-value adder in response to said reference signal or alternatively the output signal of said variable divider and then provides the hold value to said first L-value adder as the other input, and wherein the second L-value accumulator comprises: a second L-value adder that receives the value K2 (K2 is an integer) as one input; and a second data latch that holds an output of said second L-value adder in response to said reference signal or alternatively the output signal of said variable divider and then provides the hold value to said second L-value adder as the other input.

[3] A delta-sigma type fraction division PLL synthesizer according to claim 1, further comprising

a second adder for subtracting the output value of said second L-value accumulator from the output value of said first L-value accumulator, comprising

n stages ranging from a first stage to a n-th stage of delta sigma sections constructed from said first L-value accumulator, said second L-value accumulator, said first adder, and said second adder, and comprising:

first through (n-1)-th differentiation circuits for differentiating an overflow signal of each of the second stage through the n-th stage delta sigma sections respectively once through n-1 times; a third adder for adding an overflow signal of said first stage delta sigma section and an output of said first through (n-1)-th differentiation circuits; and a distributor that receives an output value of said second adder having been inputted to the next stage delta sigma section, and then distributes the value into two values in such a manner that the total of the two values should equal the output value of said second adder.

[4] A delta-sigma type fraction division PLL synthesizer according to claim 2, further comprising

a second adder for subtracting the output value of said second L-value adder from the output value of said first L-value adder, comprising

n stages ranging from a first stage to a n-th stage of delta sigma sections constructed from said first L-value accumulator, said second L-value accumulator, said first adder, and said second adder, and comprising:

first through (n-1)-th differentiation circuits for differentiating an overflow signal of each of the second stage through the n-th stage delta sigma sections respectively once through n-1 times; a third adder for adding an overflow signal of said first stage delta sigma section and an output of said

first through (n-1)-th differentiation circuits; and a distributor that receives an output value of said second adder having been inputted to the next stage delta sigma section, and then distributes the value into two values in such a manner that the total of the two values should equal the output value of said second adder.